

INFORMATION DISCLOSURE STATEMENT

Complete if known

Application Number: Not Yet Assigned 10/774,882

Filing Date: Herewith

First Named Inventor: Kevin Kwong-Tai Chung

Group Art Unit: Not Yet Assigned 2841

Examiner Name: Not Yet Assigned T. D. W. H.

SHEET 1 OF 3

Attorney Docket Number: AI-TECH-16B

UNITED STATES PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	PATENT NUMBER	ISSUE DATE MM-DD-YYYY	FIRST NAMED INVENTOR
TD		5,950,304	09/14/1999	Khandros, et al
		5,915,170	06/22/1999	Raab, et al
		5,848,467	12/15/1998	Khandros, et al
		5,685,885	11/11/1997	Khandros, et al
		5,682,061	10/28/1997	Khandros, et al
		5,929,517	07/27/1999	DiStefano, et al
		5,861,666	01/19/1999	Bellaar
		5,347,159	09/13/1994	Khandros, et al
		5,367,764	11/29/1994	DiStefano, et al
		5,558,928	09/24/1996	DiStefano, et al
		5,548,091	08/20/1996	DiStefano, et al
		5,875,545	03/02/1999	DiStefano, et al
		5,583,321	12/10/1996	DiStefano, et al
		5,570,504	11/05/1996	DiStefano, et al
		5,148,265	09/15/1992	Khandros, et al
		5,777,379	07/07/1998	Karavakis, et al

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	DOCUMENT NUMBER	COUNTRY OR REGION	DATE OF PUBLICATION MM-DD-YYYY	FIRST NAMED INVENTOR OR APPLICANT
TD		WO 98/26476	PCT	18/06/1998	DiStefano, et al
TD		WO 98/44564	PCT	08/10/1998	DiStefano, et al

OTHER PRIOR ART - NON-PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in Capital Letters), title of the article (when appropriate), title of the item(book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
TD		CO VAN VEEN, IC Packaging And Assembly Issues For Next Generation Miniaturised Consumer Electronics, Future Fab International,, Pages 379-382 (4 Pages).
		JACK FISHER, Advancements in Multilayer Material Technology, Future Circuits International, 4 Pages
EXAMINER'S SIGNATURE	DATE CONSIDERED	
T. D. W. H.	5/28/05	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw a line through citation if citation not in conformance and reference not considered. Include a copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT

Complete if known

Application Number: Not Yet Assigned

10/774,582

Filing Date: Herewith

First Named Inventor: Kevin Kwong-Tai Chung

Group Art Unit: Not Yet Assigned

241

Examiner Name: Not Yet Assigned

T. D. Wu

SHEET 2 OF 3

Attorney Docket Number: AI-TECH-16B

UNITED STATES PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	PATENT NUMBER	ISSUE DATE MM-DD-YYYY	FIRST NAMED INVENTOR
TD		5,371,654	12/06/1994	Beaman et al.
		3,555,364	01/12/1971	Matcovich
		5,798,564	08/25/1998	Eng et al.
		5,043,794	08/27/1991	Tai et al.
		4,734,825	03/29/1988	Peterson
		5,734,555	03/31/1998	McMahon
		5,943,213	08/24/1999	Sasov
		5,394,303	02/28/1995	Yamaji
		5,926,369	07/20/1999	Ingraham et al.
		5,386,341	01/31/1995	Olson et al.
		5,801,439	09/01/1998	Fujisawa et al.
		5,375,041	12/20/1994	McMahon

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	DOCUMENT NUMBER	COUNTRY OR REGION	DATE OF PUBLICATION MM-DD-YYYY	FIRST NAMED INVENTOR OR APPLICANT

OTHER PRIOR ART - NON-PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in Capital Letters), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
TD		PETRI SAVOLAINEN, <u>Area Array Packages And High-Density Printed Wiring Boards</u> , Future Circuits International, Pages 193-195 (3 Pages).
		PATRICK THOMPSON, <u>Chip-scale Packaging</u> , IEEE Spectrum, August 1997, Pages 36-43 (8 Pages).
		DENNIS HERRELL, <u>Power to the Package</u> , IEEE Spectrum, July 1999, Pages 46-53 (8 Pages).
		VERN SOLBERG, <u>Chip-Scale Array Devices</u> , Future Circuits International, 5-Pages.
		JOAN TOURNÉ, <u>The Future Of Non-Woven Laminates</u> , Future Circuits International, Pages 129-131 (3 Pages).
		WALTER OLBRICH, <u>High Density Printed Circuit Board Technologies</u> , Future Circuits International, Pages 133-138 (6 Pages).
		IVAN HO, <u>Microvia Technology</u> , Future Circuits International, Pages 139-141 (3 Pages).

EXAMINER'S SIGNATURE	DATE CONSIDERED
Tuan D. M.	5-26-05

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw a line through citation if citation not in conformance and reference not considered. Include a copy of this form with next communication to applicant.

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Filing Date: Herewith

First Named Inventor: Kevin Kwong-Tai Chung

Group Art Unit: Not Yet Assigned 2841

Examiner Name: Not Yet Assigned T. Dill

SHEET 3 OF 3

Attorney Docket Number: AI-TECH-16B

UNITED STATES PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	PATENT NUMBER	ISSUE DATE MM-DD-YYYY	FIRST NAMED INVENTOR
TD		5,192,716	03/09/1993	Jacobs
		5,794,330	08/18/1998	DiStefano, et al
		5,901,041	05/04/1999	Davies et al
		5,783,870	07/21/1998	Mostafazadeh et al
		5,672,548	09/30/1997	Culnane et al
		5,686,699	11/11/1997	Chu et al
		5,172,303	12/15/1992	Bernardoni et al
		5,286,926	02/15/1994	Kimura et al

FOREIGN PATENT DOCUMENTS

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TD		DIETER BERGMAN, BGAs The Component Package Of Choice, Future Circuits International, 7 Pages.
		MARK HUTTON, High Density Substrates for IC Packaging, Future Circuits International, 3 Pages.
		RAVI M. BHATKAL, Techno-Economic Analysis of Alternative Wafer Bumping Technologies, Future Circuits International, 4 Pages.
		International Search Report, PCT/US00/13077, 18 August 2000 (2 Pages)

EXAMINER'S SIGNATURE	DATE CONSIDERED
Tuan B. N.	5-26-08

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw a line through citation if citation not in conformance and reference not considered. Include a copy of this form with next communication to applicant.